BUILT IN SELF TEST CIRCUIT FOR MEASURING TOTAL TIMING UNCERTAINTY IN A DIGITAL DATA PATH

ABSTRACT OF THE INVENTION

[0043] A circuit for measuring timing uncertainty in a clocked digital path and in particular, the number of logic stages completed in any clock cycle. A local clock buffer receives a global clock and provides a complementary pair of local clocks. A first local (launch) clock is an input to a delay line, e.g., 3 clock cycles worth of series connected inverters. Delay line taps (inverter outputs) are inputs to a register that is clocked by the complementary clock pair to capture progression of the launch clock through the delay line and identify any variation (e.g., from jitter, VDD noise) in that progression. Global clock skew and across chip gate length variation can be measured by cross coupling launch clocks from a pair of such clock buffers and selectively passing the local and remote launch clocks to the respective delay lines.